BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

ECE-322
Electronic Circuits (B)

Lecture #9
CAD Fundamentals

Instructor:
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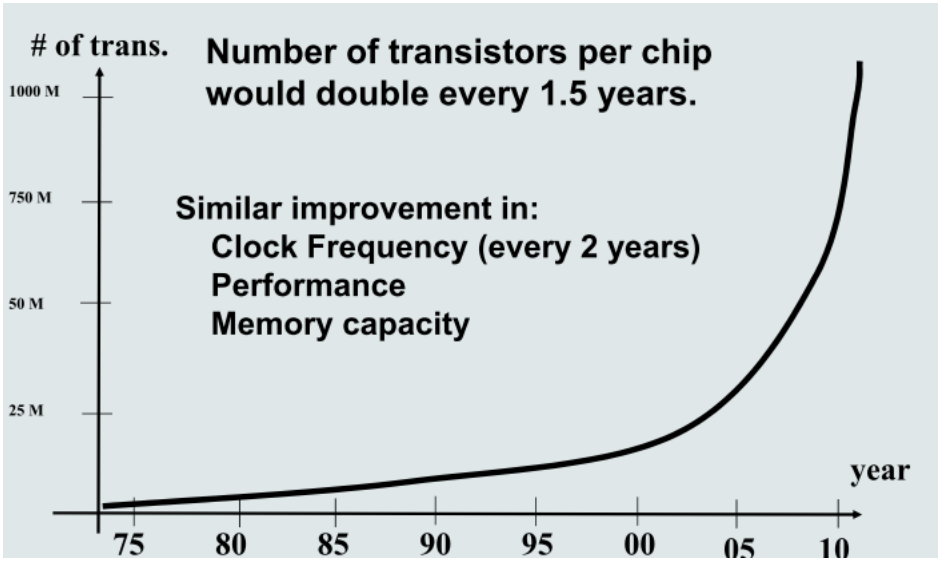
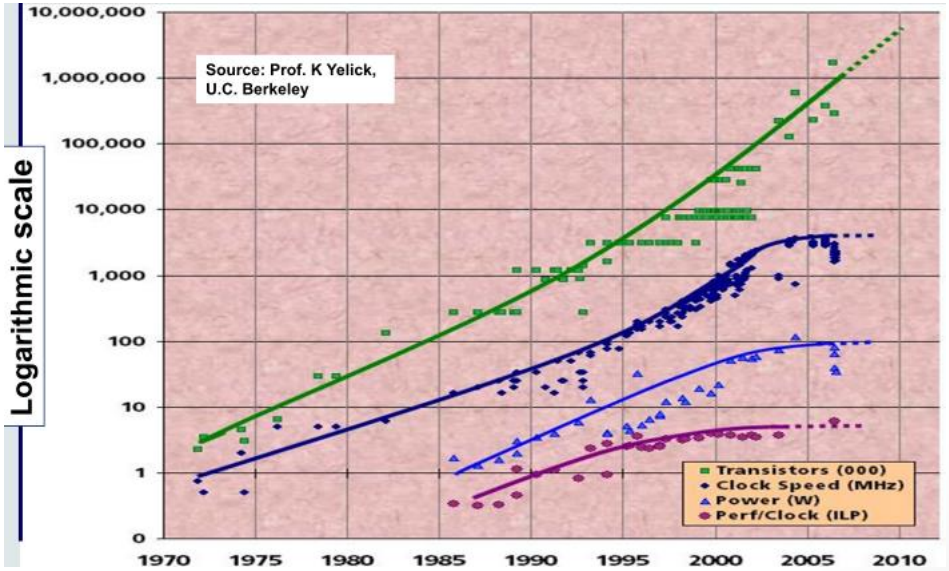
Agenda

- Trend in microelectronics
- The design challenges
- Different design paradigms
- The test problems
- Intro. to the IDE

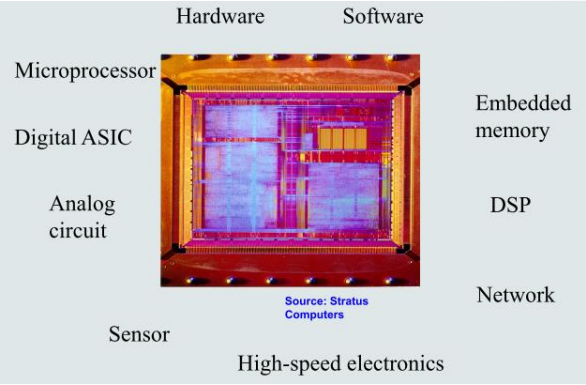
TREND IN MICROELECTRONICS

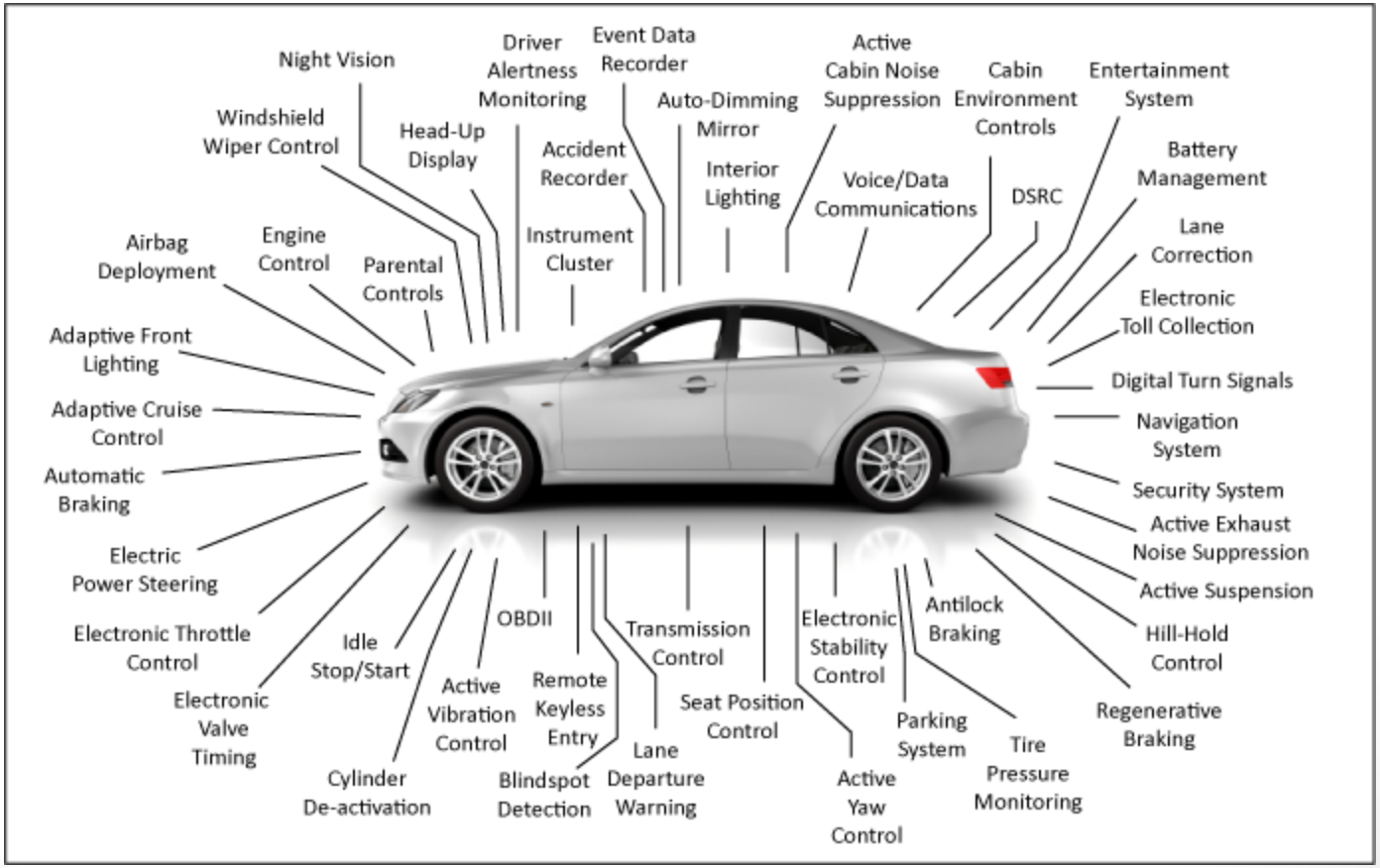
Moore's Law


# of trans.
1000 M
750 M
50 M
25 M
Number of transistors per chip would double every 1.5 years.
Similar improvement in:
Clock Frequency (every 2 years)
Performance
Memory capacity
year
75
80
85
90
95
00
05
10


Source: Prof. K Yelick, U.C. Berkeley
Logarithmic scale
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
0
1970
1975
1980
1985
1990
1995
2000
2005
2010
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)

System on Chip & System of Systems





THE DESIGN CHALLENGES

Many Design Tasks

- System specification (functionality and requirements)
- Hardware/software trade-offs
- Architecture selection and exploration
- Analysis and simulation
- Synthesis and optimization
- Implementation
- Testing and design for testability
- Verification and validation
- Design management: cooperation between tools, design flow, etc.

Design Objectives

- Unit cost: the cost of manufacturing each copy of the system, excluding NRE cost.
- NRE cost (Non-Recurring Engineering cost): The one-time cost of designing the system.
- Size: the physical space required by the system.
- Performance: the execution time or throughput .
- Power: the amount of power consumed by the system.
- Testability: the easiness of testing the system to make sure that it works correctly.
- Flexibility: the ability to change the functionality of the system without incurring heavy NRE cost.
- Correctness, safety, etc.

The Main Challenges

- System complexity
- Increasing functionality and diversity
- Increasing performance
- Stringent design requirements
- Low cost and low power
- Dependability: reliability, safety and security
- Testability and flexibility
- Technology challenges for cost-efficient implementation
- Deep submicron effects (e.g., cross talk and soft errors)

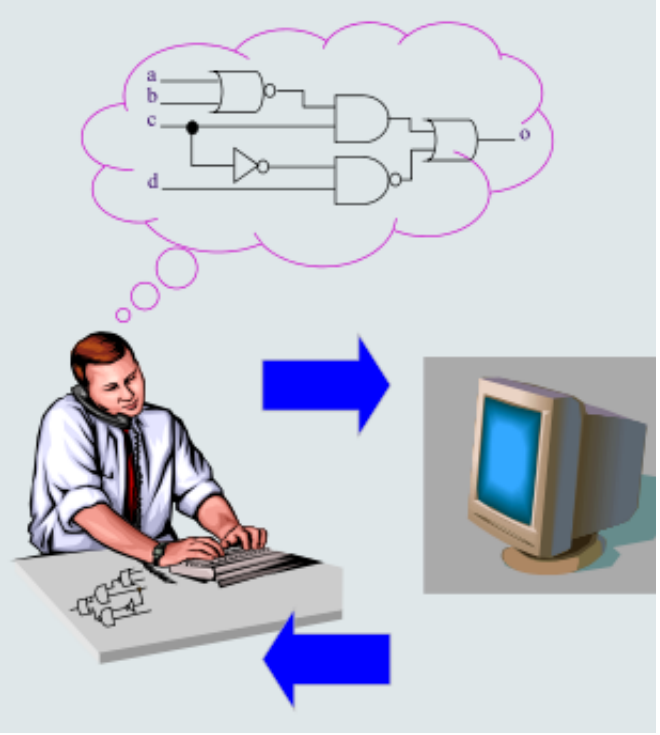
Possible Solutions:

- Powerful design methodology and CAD tools.
- Advanced architecture (modularity).
- Extensive design reuse.

DIFFERENT DESIGN PARADIGMS

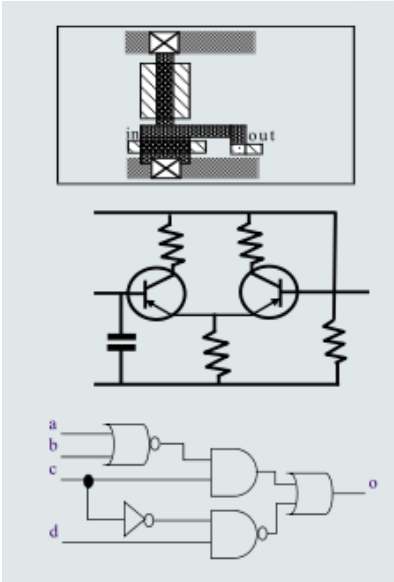
Capture and Simulate

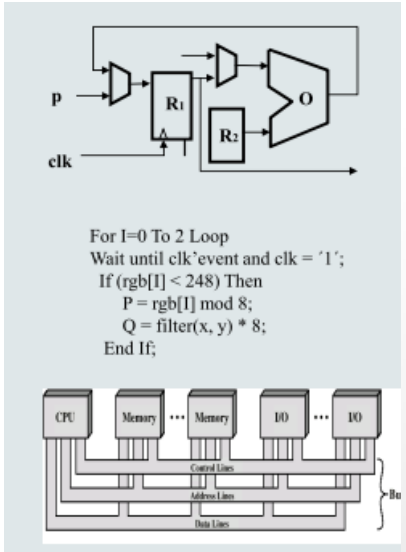
- The detailed design is captured in a **model**.
- The model is simulated.
- The results are used to guide the improvement of the design.
- All design decisions are made by the designers.



Abstraction Hierarchy

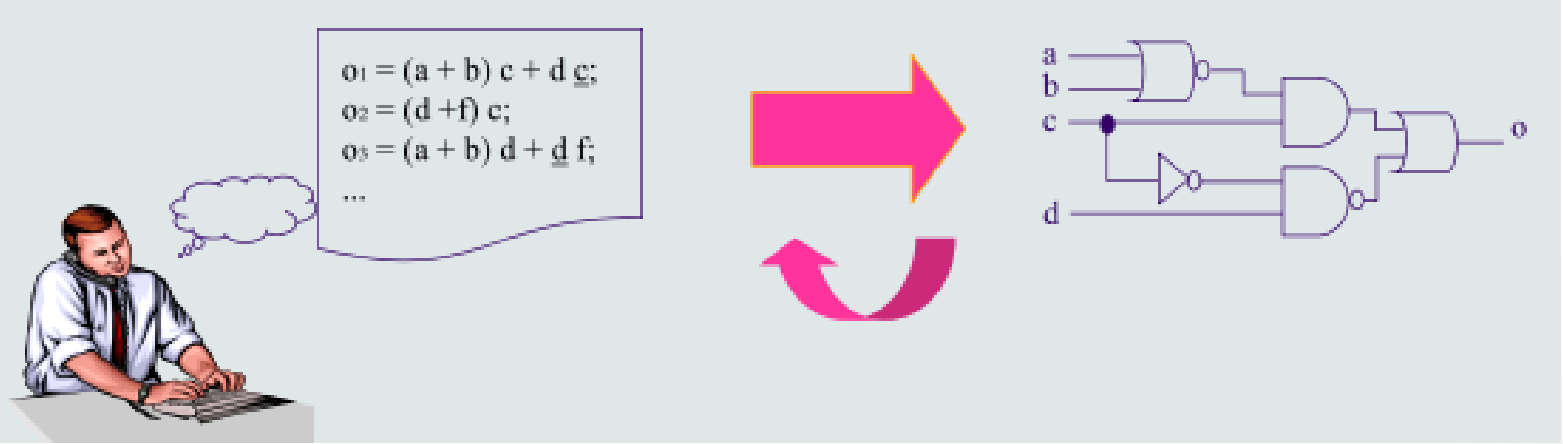
- **Layout/silicon level** : The physical layout of the integrated circuits is described.
- **Circuit level** : The detailed circuits of transistors, resistors, and capacitors are described.
- **Logic (gate) level** : The design is given as gates and their interconnections.
- **Register-transfer level (RTL)** : Operations are described as transfers of values between registers.
- **Algorithmic level** : A system is described as a set of usually concurrent algorithms.
- **System level** : A system is described as a set of processors and communication channels.





Describe and Synthesize Paradigm

- Description of a design in terms of **behavioral** specification.
- Refinement of the design towards an implementation by adding **structural** details.
- Evaluation of the design in terms of a cost function and the design is optimized w.r.t. the cost function.



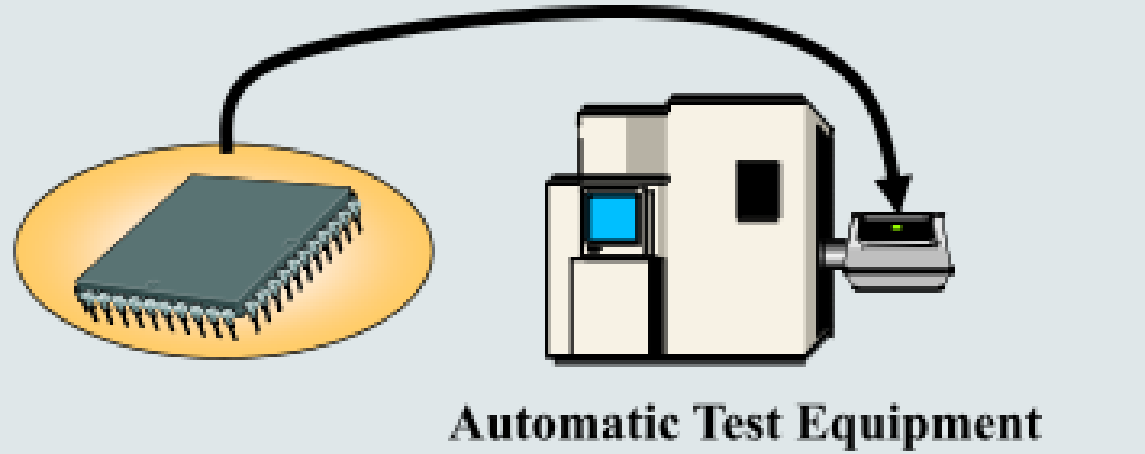
Other Paradigms

- Y-Chart
  - Behavioral, structure & physical domain
- Core-based Design
  - Reuse of IP blocks e.g. CPU, DSP,…
- Platform-based Design
  - Customized embedded processors or software

THE TEST PROBLEMS

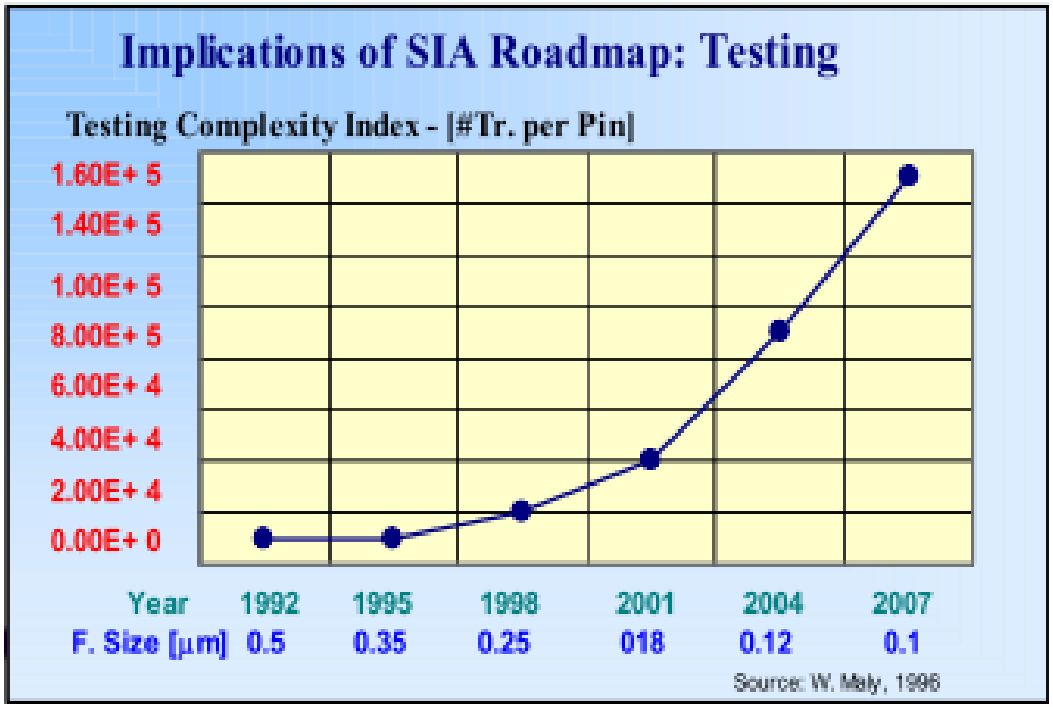
Testing and its Current Practice

- Testing aims at the detection of physical faults (production errors/defects and physical failures).
- Different from the design task, testing is performed on each individual chip, after it is manufactured (volume sensitive).
- The common approach to perform testing is to utilize an Automatic Test Equipment (ATE).



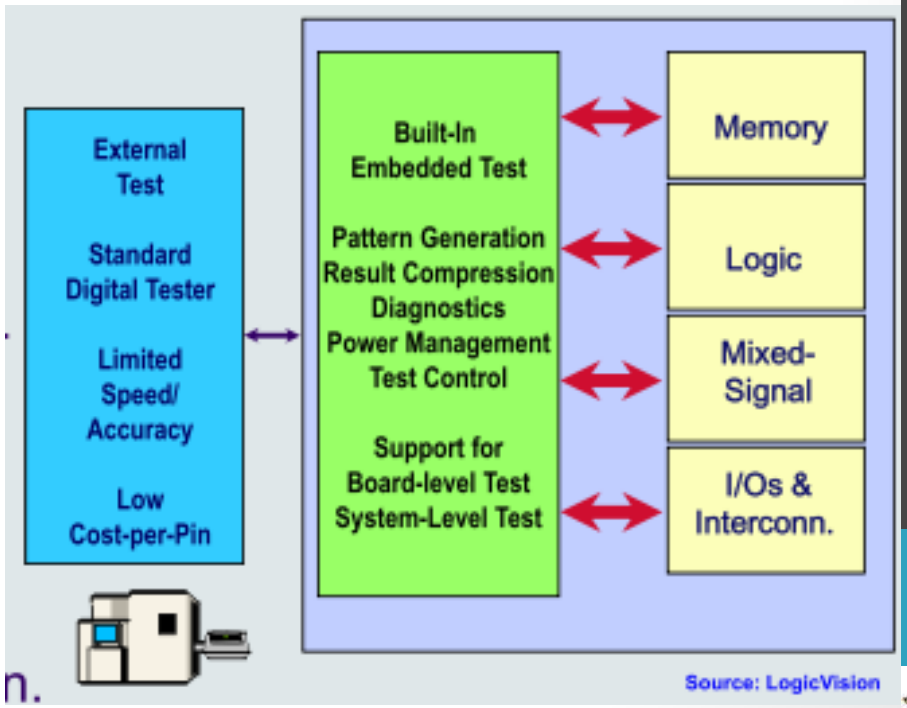
High Test Complexity

- # of transistors increases exponentially.
- # of access port remains stable.
- Implication:
  - Test Complexity Index (# of transistors per pin) increases rapidly.



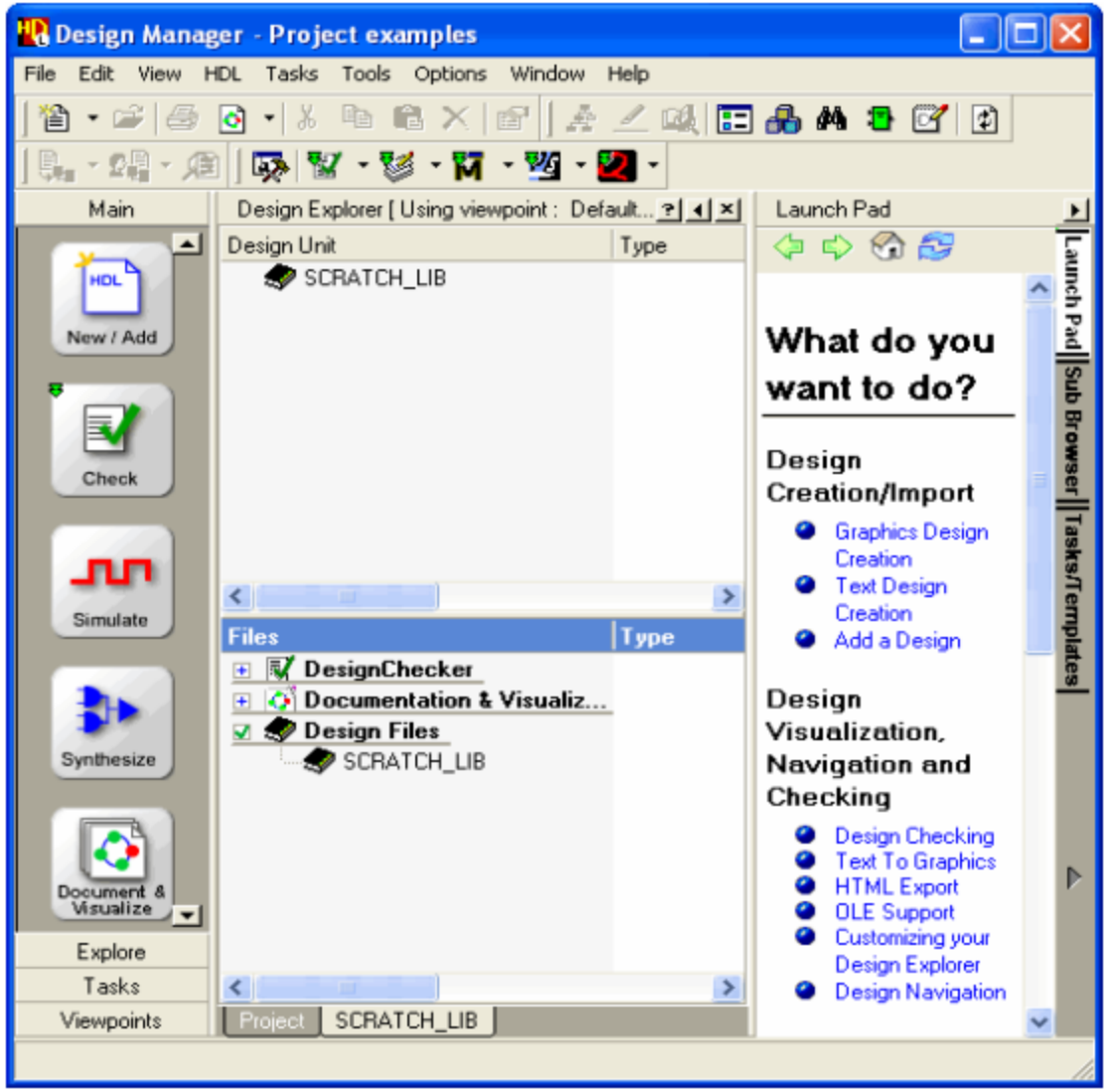
Built-In Self Test (BIST)

- Solution: Dedicated built-in hardware for implementing test functions.
  - No need for expensive ATE.
  - Speed testing.
  - Concurrent test possible.
  - Support field test and diagnosis

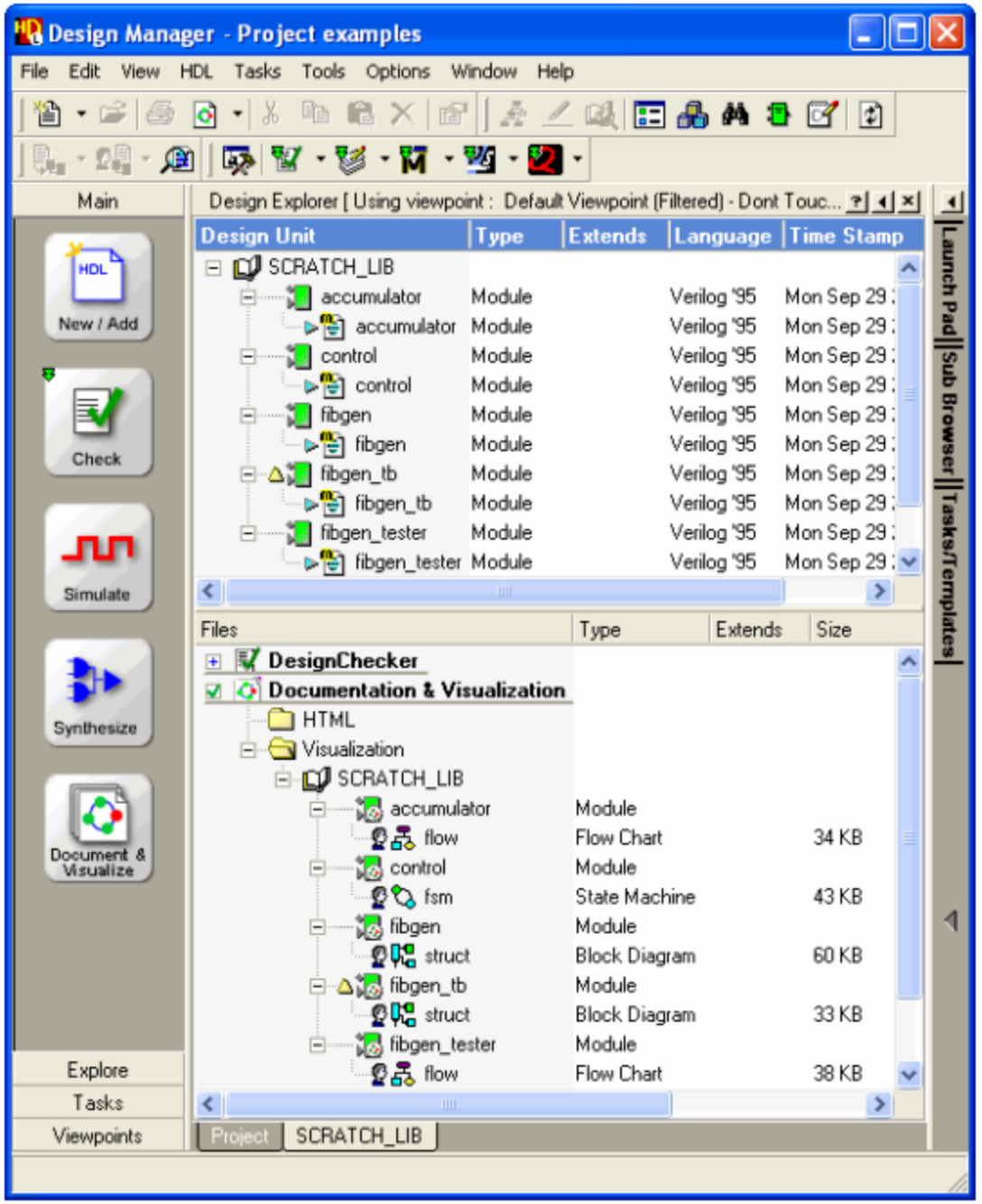


A FIRST LOOK ON THE IDE

The Design Manager



Browse a design



Tasks

- Install the suitable IDE to you
  - Xilinx ISE®
  - FPGA Advantage ®
  - Open Source tools
    - qucs (Quite Universal Circuit Simulator)
    - ChipVault
    - …
    - find more @ http://www.vlsiacademy.org/open-source-cad-tools.html
- Create a new project.
- Develop & Simulate basic logic gates e.g AND, OR, XOR, ….

- For more details, refer to:
  - **Computer Aided Design of Electronics** *course lecture notes*.
  - **The VHDL Cookbook**, *Peter J. Ashenden, 1st edition, 1990.*
- The lecture is available online at:
  - http://bu.edu.eg/staff/ahmad.elbanna-courses/12135
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg